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**REVISION HISTORY**

Version	Date	Page (New)	Section	Description
Ver 3.0	Sep.24,'05	All	All	Approval specification was first issued
Ver 3.1	Dec.12'05	P19	6.2	Marked t7 at drawing
		P21	7.2	Modified tolerance of white color chromaticity



1. GENERAL DESCRIPTION

1.1 OVERVIEW

N150X3- L09 is a 15.0" TFT Liquid Crystal Display module & ROHS module. This module supports 1024 x 768 XGA mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction.

1.2 FEATURES

- Thin and Light Weight
- XGA (1024 x 768 pixels) resolution
- DE only mode
- 3.3V LVDS (Low Voltage Differential Signaling) interface with 1 pixel/clock
- SPWG (Standard Panel Working Group) Style B compatible
- Single CCFL

1.3 APPLICATION

- TFT LCD Notebook

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	304.1 (H) x 228.1 (V) (15.0" diagonal)	mm	(1)
Bezel Opening Area	307.8 (H) x 231.6 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1024 x R.G.B. x 768	pixel	-
Pixel Pitch	0.297 (H) x 0.297 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hardness (2H), Haze 40, Reflection $\leq 3\%$	-	-

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	316.8	317.3	317.8	mm	(1)
	Vertical(V)	241.5	242	242.5	mm	(1)
	Depth(D)	-	5.7	6.0	mm	(1)
Weight		-	500	515	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.



2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	+50	°C	(1), (2)
Shock (Non-Operating)	S _{NOP}	-	210	G	(3), (5)
Vibration (Non-Operating)	V _{NOP}	-	1.5	G	(4), (5)

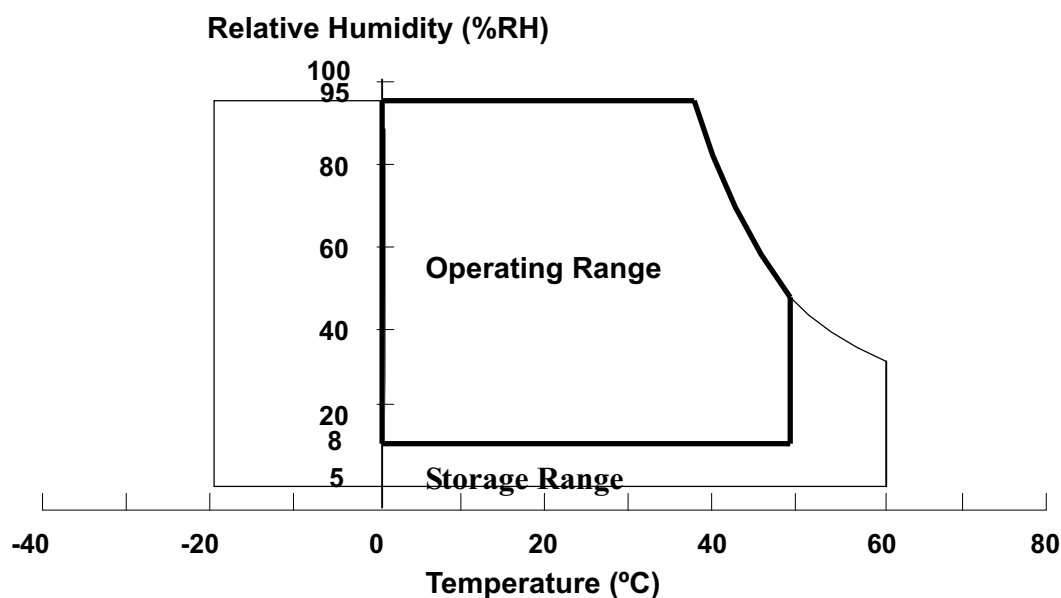
Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. ($T_a \leq 40\text{ }^{\circ}\text{C}$).

(b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40\text{ }^{\circ}\text{C}$).

(c) No condensation .

Note (2) The temperature of panel display surface area should be 0 °C Min. and 60 °C Max.



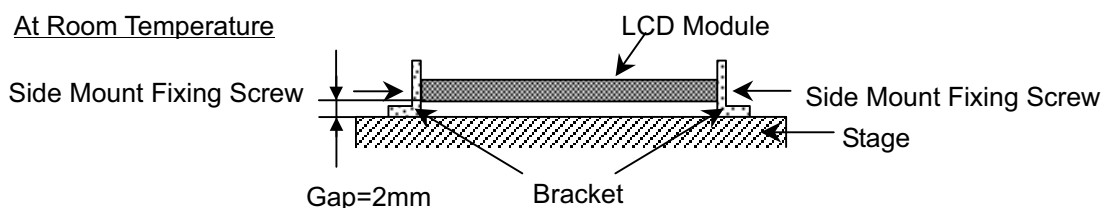
Note (3) 1 time for $\pm X, \pm Y, \pm Z$. for Condition (210G / 3ms) is half Sine Wave,

Condition(50G / 18ms) is Rectangle Wave,

Note (4) 10 ~ 200 Hz, 0.5 Hr / Cycle, 1 cycles for each X, Y, Z.:

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

The fixing condition is shown as below:





2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	$V_{CC}+0.3$	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_L	-	2.5K	V_{RMS}	(1), (2), $I_L = 6.0 \text{ mA}$
Lamp Current	I_L	2	7	mA_{RMS}	
Lamp Frequency	F_L	45	80	KHz	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to 3.2 for further information).

3. ELECTRICAL CHARACTERISTICS

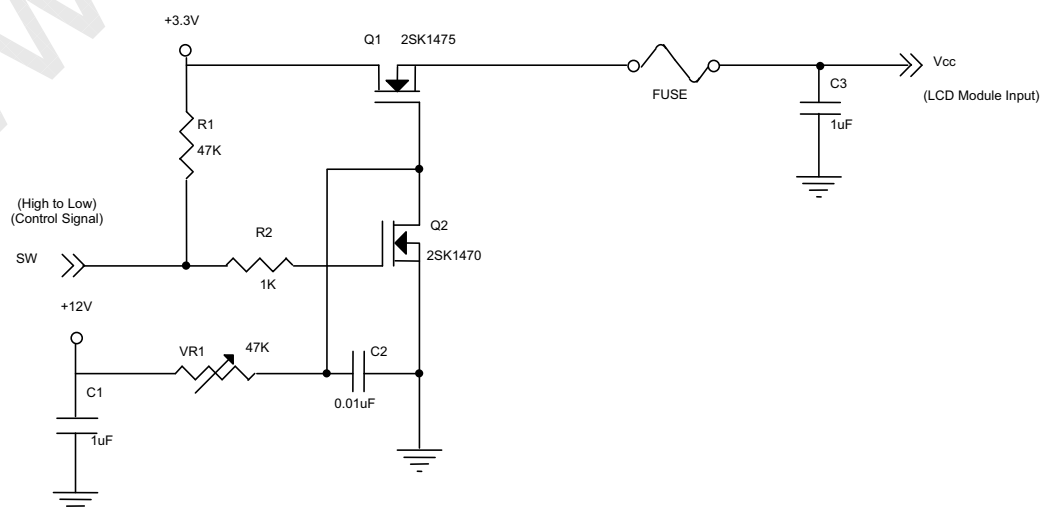
3.1 TFT LCD MODULE

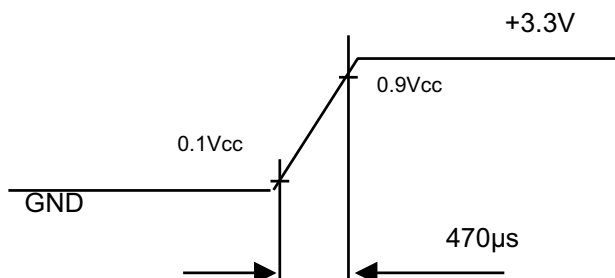
$T_a = 25 \pm 2^\circ \text{C}$

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	3.0	3.3	3.6	V	-
Ripple Voltage		V_{RP}	-	100	-	mV	-
Rush Current		I_{RUSH}	-	-	1.5	A	(2)
Power Supply Current	White	I_{CC}	-	300	350	mA	(3)a
	Black		-	350	400	mA	(3)b
Logical Input Voltage (LVDS)	"H" Level	V_{IL}	-	-	+100	mV	-
	"L" Level	V_{IH}	-100	-	-	mV	-
Terminating Resistor		R_T	-	100	-	Ohm	-
Power per EBL WG		P_{EBL}	-	3.176	-	W	(4)

Note (1) The module should be always operated within above ranges.

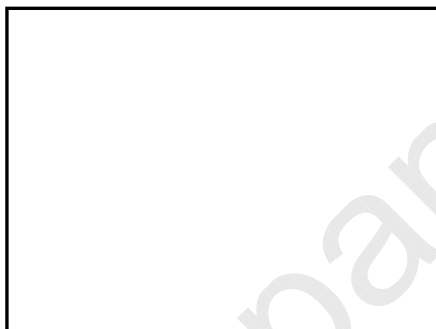
Note (2) Measurement Conditions:




Vcc rising time is 470μs


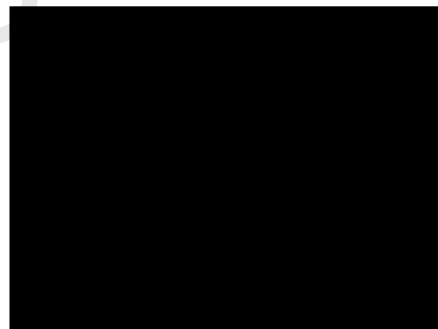
Note (3) The specified power supply current is under the conditions at $V_{cc} = 3.3\text{ V}$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, $f_v = 60\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. White Pattern



Active Area

b. Black Pattern



Active Area

Note (4) The specified power are the sum of LCD panel electronics input power and the inverter input power. Test conditions are as follows.

- (a) $V_{cc} = 3.3\text{ V}$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, $f_v = 60\text{ Hz}$,
- (b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.
- (c) Luminance: 60 nits.
- (d) The inverter used is provided from O2Micro (www.o2micro.com). Please contact O2Mirco for detail information. CMO doesn't provide the inverter in this product.

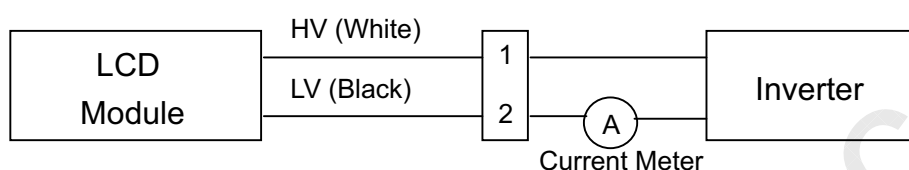


3.2 BACKLIGHT UNIT

 $T_a = 25 \pm 2^\circ\text{C}$

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	627	660	693	V_{RMS}	$I_L = 6.0\text{ mA}$
Lamp Current	I_L	2.0	6.0	6.5	mA_{RMS}	(1)
Lamp Turn On Voltage	V_s	---	---	1110 (25 °C)	V_{RMS}	(2)
		---	---	1330 (0 °C)	V_{RMS}	(2)
Operating Frequency	F_L	45	60	80	KHz	(3)
Lamp Life Time	L_{BL}	15000	---	-	Hrs	(5)
Power Consumption	P_L	-	3.96	-	W	(4), $I_L = 6.0\text{ mA}$

Note (1) Lamp current is measured by utilizing a high frequency current meter as shown below:



Note (2) The voltage shown above should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) $P_L = I_L \times V_L$

Note (5) The lifetime of lamp can be defined as the time in which it continues to operate under the condition $T_a = 25 \pm 2^\circ\text{C}$ and $I_L = 6.0\text{ mA}_{RMS}$ until one of the following events occurs:

- (a) When the brightness becomes or lower than 50% of its original value.
- (b) When the effective ignition length becomes or lower than 80% of its original value. (Effective ignition length is defined as an area that has less than 70% brightness compared to the brightness in the center point.)

Note (6) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid producing too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

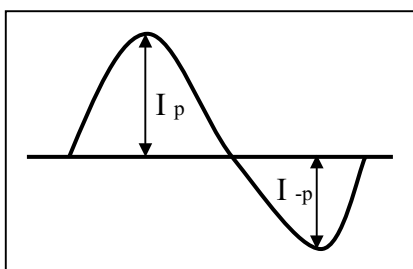


The output of the inverter must have symmetrical (negative and positive) voltage waveform and symmetrical current waveform. (Unsymmetrical ratio is less than 10%) Please do not use the inverter which has unsymmetrical voltage and unsymmetrical current and spike wave. Lamp frequency may produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

- The asymmetry rate of the inverter waveform should be 10% below;
- The distortion rate of the waveform should be within $\sqrt{2} \pm 10\%$;

The ideal sine wave form shall be symmetric in positive and negative polarities.



* Asymmetry rate:

$$|I_p - I_{-p}| / I_{rms} * 100\%$$

* Distortion rate

$$I_p \text{ (or } I_{-p}) / I_{rms}$$


CHI MEI
OPTOELECTRONICS CORP.

Issued Date: Dec.12, 2005

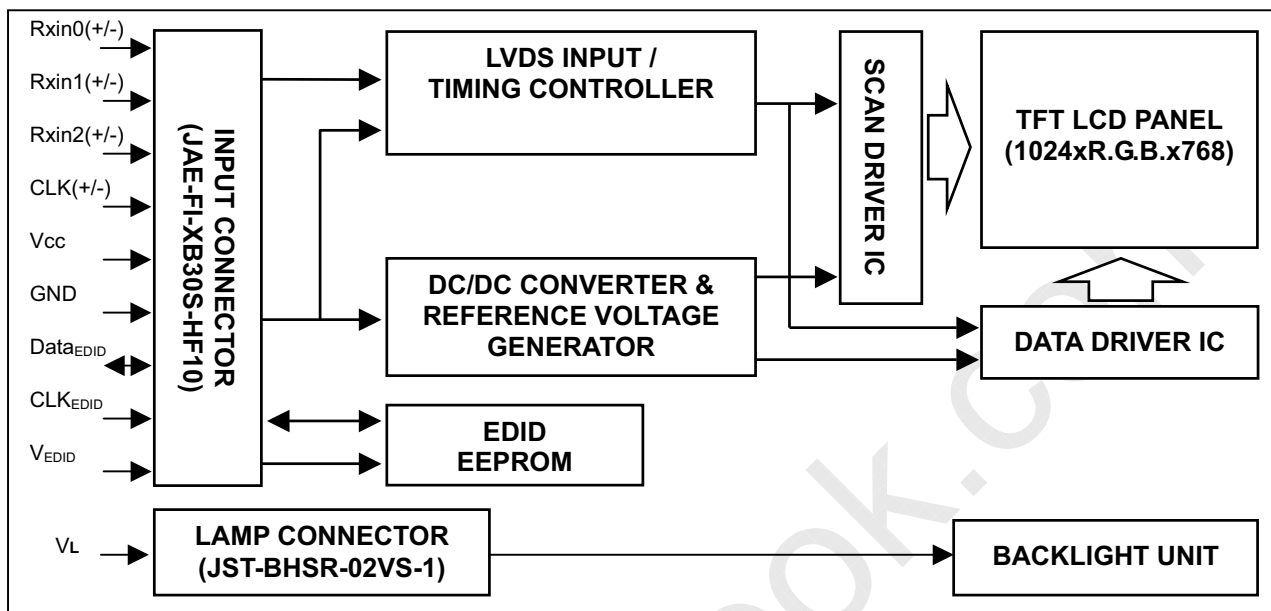
Model No.: N150X3 - L0A

Approval

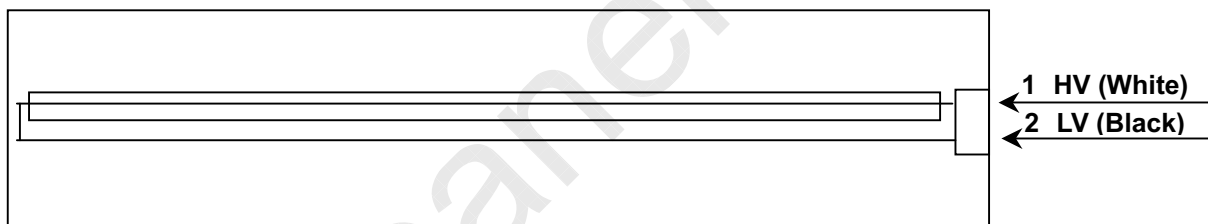
4. BLOCK DIAGRAM

TFT LCD MODULE

4.1 TFT LCD MODULE



4.2 BACKLIGHT UNIT





5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

Pin	Symbol	Description	Polarity	Remark
1	Vss	Ground		
2	Vcc	Power Supply +3.3 V (typical)		
3	Vcc	Power Supply +3.3 V (typical)		
4	V _{EDID}	DDC 3.3V Power		DDC 3.3V Power
5	NC	Non-Connection		
6	CLK _{EDID}	DDC Clock		DDC Clock
7	DATA _{EDID}	DDC Data		DDC Data
8	Rxin0-	LVDS Differential Data Input	Negative	R0~R5,G0
9	Rxin0+	LVDS Differential Data Input	Positive	
10	Vss	Ground		
11	Rxin1-	LVDS Differential Data Input	Negative	G1~G5,B0,B1
12	Rxin1+	LVDS Differential Data Input	Positive	
13	Vss	Ground		
14	Rxin2-	LVDS Differential Data Input	Negative	B2~B5,DE,Hsync,Vsync
15	Rxin2+	LVDS Differential Data Input	Positive	
16	Vss	Ground		
17	CLK-	LVDS Clock Data Input	Negative	LVDS Level Clock
18	CLK+	LVDS Clock Data Input	Positive	
19	Vss	Ground		
20	NC	Non-Connection		
21	NC	Non-Connection		
22	Vss	Ground		
23	NC	Non-Connection		
24	NC	Non-Connection		
25	Vss	Ground		
26	NC	Non-Connection		
27	NC	Non-Connection		
28	Vss	Ground		
29	NC	Non-Connection		
30	NC	Non-Connection		

Note (1) Connector Part No.: JAE-FI-XB30SL-HF10

Note (2) User's connector Part No: JAE-FI-X30C2L

Note (3) The first pixel is even.

5.2 BACKLIGHT UNIT

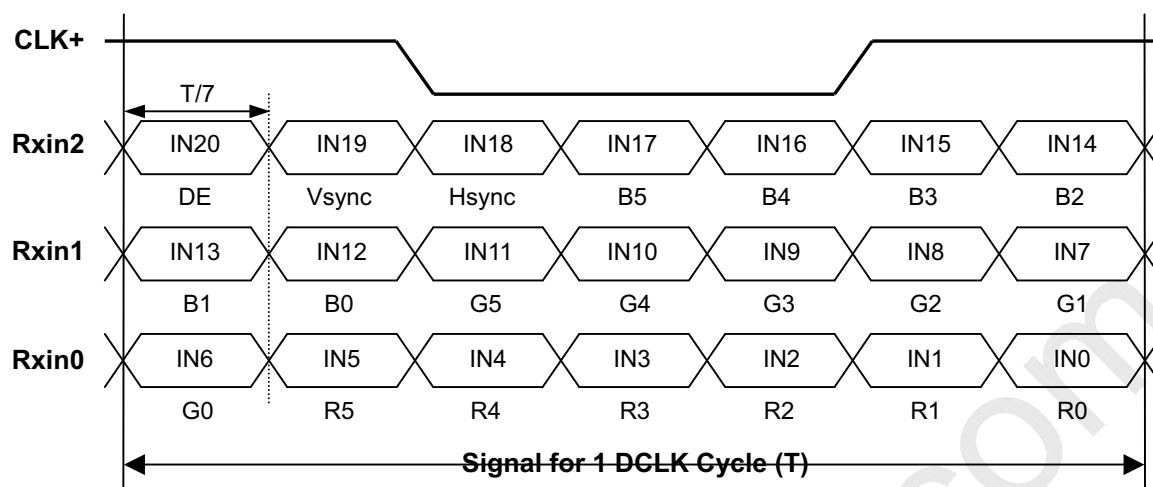
Pin	Symbol	Description	Color
1	HV	High Voltage	White
2	LV	Ground	Black

Note (1) Connector Part No.: JST-BHSR-02VS-1

Note (2) User's connector Part No.: JST-SM02B-BHSS-1-TB



5.3 TIMING DIAGRAM OF LVDS INPUT SIGNAL





5.4 EDID DATA

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPD1 standards.

Byte # (decimal)	Byte #(hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header , Fixed	00	00000000
1	1	Header , Fixed	FF	11111111
2	2	Header , Fixed	FF	11111111
3	3	Header , Fixed	FF	11111111
4	4	Header , Fixed	FF	11111111
5	5	Header , Fixed	FF	11111111
6	6	Header , Fixed	FF	11111111
7	7	Header , Fixed	00	00000000
8	8	ID=IBM	30	00100100
9	9	ID=IBM	AE	01001101
10	0A	XGA (IBM Unique ID)	40	01010101
11	0B	XGA (IBM Unique ID)	40	00001010
12	0C	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
13	0D	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
14	0E	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
15	0F	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
16	10	Week of manufacture 1 - 53 (unused: 00h)	32	00000000
17	11	Year of manufacture year - 1990(unsed:00h)	0F	00000000
18	12	Version=1	01	00000001
19	13	Revision=3	03	00000011
20	14	Digital	80	10000000
21	15	Active area horizontal 30.4128 cm	1E	00011110
22	16	Active area vertical 22.8096cm	17	00010111
23	17	gamma * 100-100 = 2.2*100-100=120	78	01111000
24	18	Feature support (no DPMS, Active off, RGB, Preferred Timing Mode)	EA	00001010
25	19	Rx1 Rx0 Ry1 Ry0 Gx1 Gx0 Gy1 Gy0	77	01110111
26	1A	Bx1 Bx0 By1 By0 Wx1 Wx0 Wy1 Wy0	F1	11110001
27	1B	Rx=0.626	A0	10100000
28	1C	Ry=0.355	5A	01011010
29	1D	Gx=0.294	4B	01001011
30	1E	Gy=0.589	96	10010110
31	1F	Bx=0.144	24	00100100
32	20	By=0.097	18	00011000
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	21	00000000
36	24	Established timings 2 (1024x768@60Hz)	08	00001000
37	25	No manufacturer's specific timing	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001



41	29	Standard timing ID # 2	01	00000001
42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("65MHz")	64	01100100
55	37	65MHz/10000 =6500=1964H	19	00011001
56	38	HActive(D7-D0) = 1024 mod 256	00	00000000
57	39	HBlank(D7-D0) = 320 mod 256	40	01000000
58	3A	HActive(D11-D8) : HBlank(D11-D8) = 1024/256 : 320/256	41	01000001
59	3B	VActive(D7-D0) = 768 mod 256	00	00000000
60	3C	VBlank(D7-D0) = 38 mod 256	26	00100110
61	3D	VActive(D11-D8) : VBlank(D11-D8) = 768/256 : 38/256	30	00110000
62	3E	HSyncOffset(D7-D0) = HBorder+HFrontPorch = 24	18	00011000
63	3F	HSyncWidth(D7-D0) = 136	88	10001000
64	40	VSyncoffset(D3-D0)=3 : VSyncoffset(D3-D0)=6	36	00110110
65	41	HSyncoffset(D9-D8) : HSyncoffset(D9-D8) : VSyncoffset(D5-D4) : VSyncoffset(D5-D4)	00	00000000
66	42	HImageSize(mm, D7-D0) = 304mod 256	30	00110000
67	43	VImageSize(mm, D7-D0) = 228mod 256	E4	11100100
68	44	HImageSize(D11-D8) : VImageSize(D11-D8) = 304/256 : 228/256	10	00010000
69	45	Horizontal Border=0	00	00000000
70	46	Vertical Border=0	00	00000000
71	47	Non-interlaced, Normal Display, Digital separate, Positive Hsync, Negative Vsync	18	00011000
72	48	Detailed timing description # 1 Pixel clock ("54.16MHz")	28	01010000
73	49	54.16MHz/10000 =5416=1528H	15	00010100
74	4A	HActive(D7-D0) = 1024 mod 256	00	00000000
75	4B	HBlank(D7-D0) = 320 mod 256	40	00100000
76	4C	HActive(D11-D8) : HBlank(D11-D8) = 1024/256 : 320/256	41	01000001
77	4D	Vertical Active =768 mod 256	00	00000000
78	4E	Vertical Blanking =38 mod 256	26	00011001
79	4F	VActive(D11-D8) : VBlank(D11-D8) = 768/256 : 38/256	30	00110000
80	50	HSyncOffset(D7-D0) = HBorder+HFrontPorch = 24	18	00101000
81	51	HSyncWidth(D7-D0) = 136	88	01101000
82	52	VSyncoffset(D3-D0)=3 : VSyncoffset(D3-D0)=6	36	00110100
83	53	Horizontal Vertical Sync Offset/Width upper 2bits = 0	00	00000000
84	54	HImageSize(mm, D7-D0) = 304mod 256	30	00011101
85	55	VImageSize(mm, D7-D0) = 228mod 256	E4	11010110



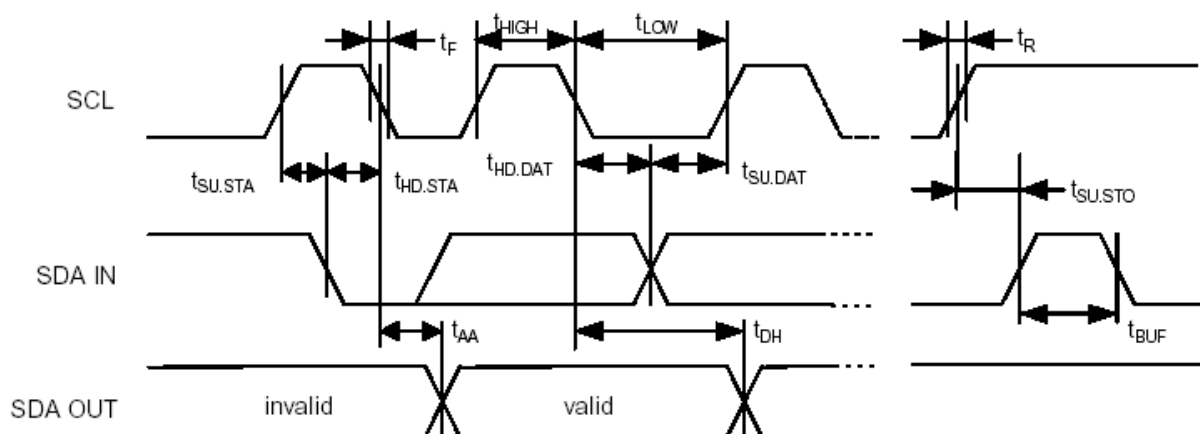
86	56	HImageSize(D11-D8) : VImageSize(D11-D8) = 304/256 : 228/256	10	00010000
87	57	Horizontal Border=0	00	00000000
88	58	Vertical Border=0	00	00000000
89	59	Non-interlaced,Normal display,no stereo,Digital separate sync,H/V pol negatives	18	00011000
90	5A	Flag	00	00000000
91	5B	Flag	00	00000000
92	5C	Flag	00	00000000
93	5D	Data type tag :0F	0F	00001111
94	5E	Flag	00	00000000
95	5F	Low Refresh Rate #1 (Horizontal active pixels / 8) - 31=97(61h)	61	01100001
96	60	Low Refresh Rate #1 Image Aspect ratio(4 : 3)	43	01000011
97	61	Low Refresh Rate #1 Refresh Rate=50Hz	32	00110010
98	62	Low Refresh Rate #2 (Horizontal active pixels / 8) - 31=97(61h)	61	01100001
99	63	Low Refresh Rate #2 Image Aspect ratio(4 : 3)	43	01000011
100	64	Low Refresh Rate #2 Refresh Rate=40Hz	28	00101000
101	65	Brightness (1/10nit) , 200/10=20(=14h)	14	00010100
102	66	Feature Flags	01	00000001
103	67	Reserved	00	00000000
104	68	EISA manufacturer code(3 Character ID) -CMO	0D	00001101
105	69	Compressed ASCII	AF	10101111
106	6A	Panel Supplier Reserved - Product code -1512	12	00010010
107	6B	(Hex, LSB first)	15	00010101
108	6C	Flag	00	00000000
109	6D	Flag	00	00000000
110	6E	Flag	00	00000000
111	6F	Data type tag : FEh	FE	11111110
112	70	Flag	00	00000000
113	71	"N"	4E	01001110
114	72	"1"	31	00110001
115	73	"5"	35	00110101
116	74	"0"	30	00110000
117	75	"X"	58	01011000
118	76	"3"	33	00110011
119	77	"_"	2D	00101101
120	78	"L"	4C	01001100
121	79	"0"	30	00110000
122	7A	"A"	41	01000001
123	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010
124	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
125	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
126	7E	No extension	00	00000000
127	7F	One-byte checksum of entire 128 bytes EDID equals 00h.	1A	00011010



5.5 EDID SIGNAL SPECIFICATION

(1) EDID Power

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply voltage	Vcc	—	2.7	—	5.5	V



(2) DC characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current Vcc=5.0V	Icc	READ at 100kHz	—	0.4	1.0	mA
Supply current Vcc=5.0V	Icc	WRITE at 100kHz	—	2.0	3.0	mA
Standby Current	ISB	Vin=Vcc or Vss	—	1.6	4.0	μA
Input Leakage Current	ILI	Vin=Vcc or Vss	—	0.1	3.0	μA
Onput Leakage Current	ILO	Vout=Vcc or Vss	—	0.05	3.0	μA
Input Low Level	VIL	—	-1.0	—	Vcc x 0.3	V
Input High Level	VIH	—	Vcc x 0.7	—	Vcc+0.5	V
Output Low Level Vcc=1.8V	VOL1	IOL=0.15mA	—	—	0.2	V
Output Low Level Vcc=3.0V	VOL2	IOL=2.1mA	—	—	0.4	V



(3) AC characteristics (VCC=2.5~5.5V standard operation mode)

Parameter	Symbol	Min	Max	Unit
Clock Frequency, SCL	F _{SCL}	—	100	kHz
Clock Pulse Width Low	T _{LOW}	4.7	—	μs
Clock Pulse Width High	T _{HIGH}	4.0	—	μs
Noise Suppression Time	T _I	—	100	ns
Clock Low to Data Out Valid	T _{AA}	0.1	4.5	μs
Time the bus must be free before a new transmission can start	T _{BUF}	4.7	—	μs
Start Hold Time	T _{HD.STA}	4.0	—	μs
Start Set-up Time	T _{SU.STA}	4.7	—	μs
Data in Hold Time	T _{HD.DAT}	0	—	μs
Data in Set-up Time	T _{SU.DAT}	200	—	ns
Inputs Rise Time	T _R	—	1.0	μs
Inputs Fall Time	T _F	—	300	ns
Stop Set-up Time	T _{SU.STO}	4.7	—	μs
Data Out Hold Time	T _{DH}	100	—	ns
Write Cycle Time	T _{WR}	—	10	ms



5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0
Blue(63)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	

Note (1) 0: Low Level Voltage, 1: High Level Voltage



6. INTERFACE TIMING

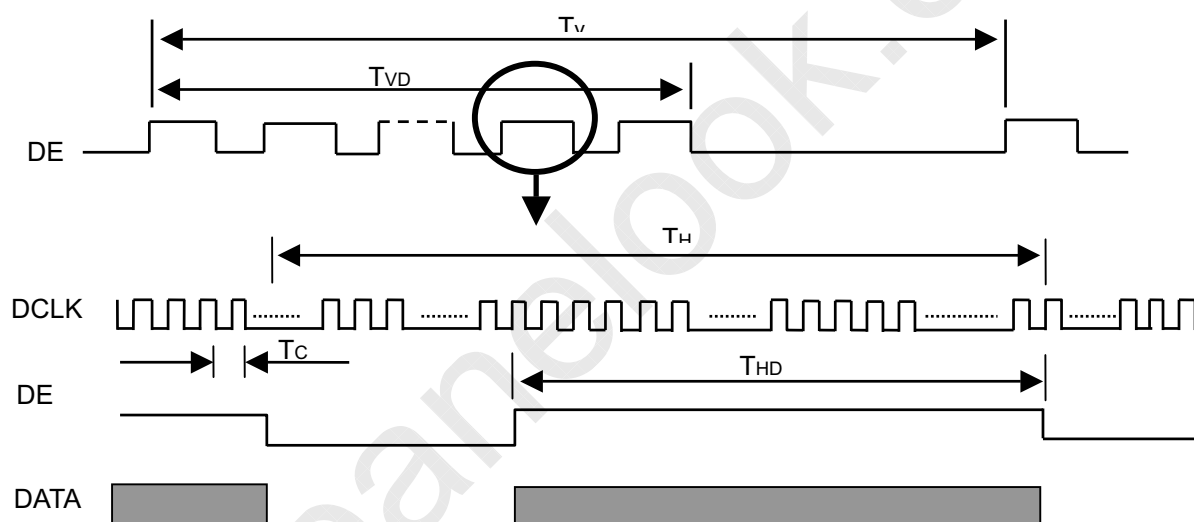
6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

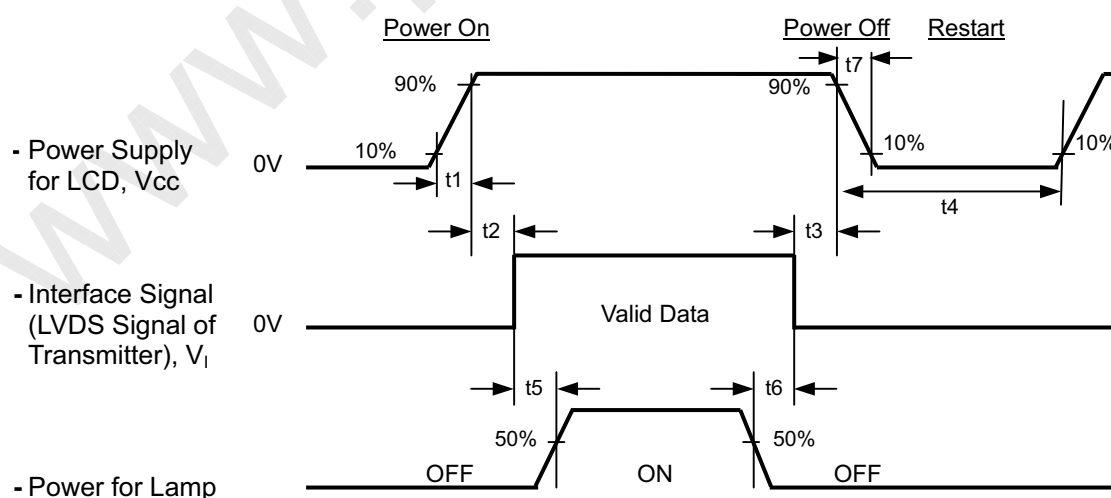
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	50	65	68	MHz	-
DE	Vertical Total Time	TV	771	806	850	TH	-
	Vertical Addressing Time	TVD	768	768	768	TH	-
	Horizontal Total Time	TH	1200	1344	1600	Tc	-
	Horizontal Addressing Time	THD	1024	1024	1024	Tc	-

Note (1) Because this module is operated by DE only mode, Hsync and Vsync input signals should be set to low logic level or ground. Otherwise, this module would operate abnormally.

INPUT SIGNAL TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE





Timing Specifications:

$$t1 \leq 10 \text{ msec}$$

$$0 < t2 \leq 50 \text{ msec}$$

$$0 < t3 \quad \text{msec}$$

$$t4 \geq 150 \text{ msec}$$

$$t5 \geq 200 \text{ msec}$$

$$t6 \geq 0 \quad \text{msec}$$

$$t7 \leq 10 \quad \text{msec}$$

Note (1) Please avoid floating state of interface signal at invalid period.

Note (2) When the interface signal is invalid, be sure to pull down the power supply of LCD Vcc to 0 V.

Note (3) The Backlight inverter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight inverter power must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Sometimes some slight noise shows when LCD is turned off (even backlight is already off). To avoid this phenomenon, we suggest that the Vcc falling time had better to follow $t7 \geq 5 \text{ msec}$



7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Inverter Current	I _L	6.0	mA
Inverter Driving Frequency	F _L	61	KHz
Inverter	Sumida H05 4915		

The relative measurement methods of optical characteristics are shown in 6.2. The following items should be measured under the test conditions described in 6.1 and stable environment shown in Note (6).

7.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	R _x	$\theta_x=0^\circ, \theta_Y=0^\circ$ CS-1000T	TYP -0.03	0.580	TYP +0.03	---	(1), (5)
		R _y			0.335		---	
	Green	G _x			0.314		---	
		G _y			0.534		---	
	Blue	B _x			0.151		---	
		B _y			0.119		---	
	White	W _x		0.285	0.313	0.341	---	
		W _y		0.309	0.329	0.349	---	
Average Luminance of White		L _{AVE}		170	200	---	cd/m ²	(4),(5)
Contrast Ratio		CR		170	250	---	---	(2), (5)
Color Gamut		C.G%		---	45	---		(5), (7)
Response Time		T _r	$\theta_x=0^\circ, \theta_Y=0^\circ$	---	5	10	ms	(3)
		T _f		---	11	16	ms	
White Variation		δW ₅	$\theta_x=0^\circ, \theta_Y=0^\circ$ CA-210	80	---	---	%	(6)
		δW ₁₃		65	---	---		
Viewing Angle	Horizontal	θ _x +	CR≥10 CA-210	40	45	---	Deg.	(1), (5)
		θ _x -		40	45	---		
	Vertical	θ _y +		15	20	---		
		θ _y -		40	45	---		



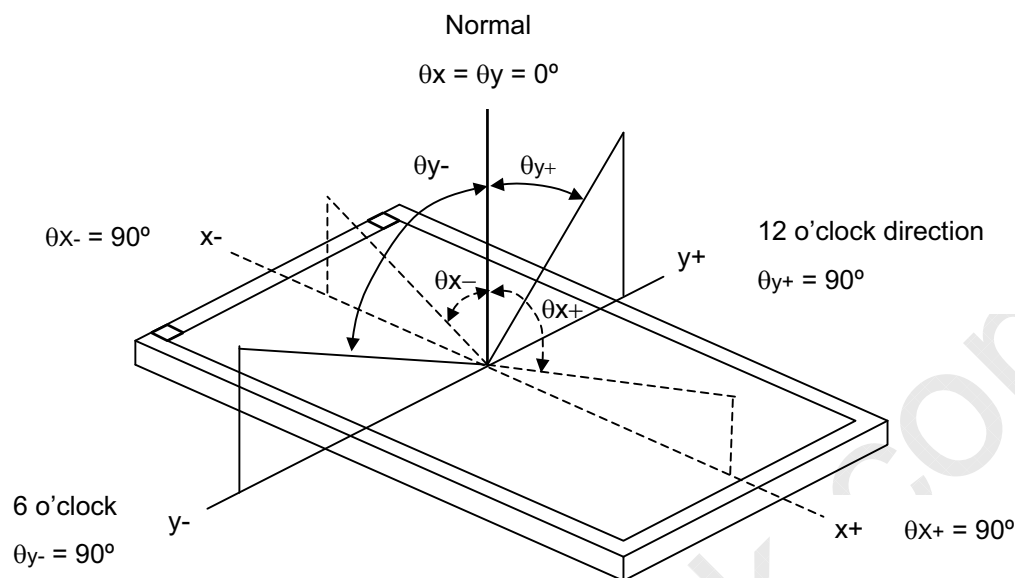
CHI MEI
OPTOELECTRONICS CORP.

Issued Date: Dec.12, 2005

Model No.: N150X3 - L0A

Approval

Note (1) Definition of Viewing Angle (θ_x , θ_y):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{63} / L_0$$

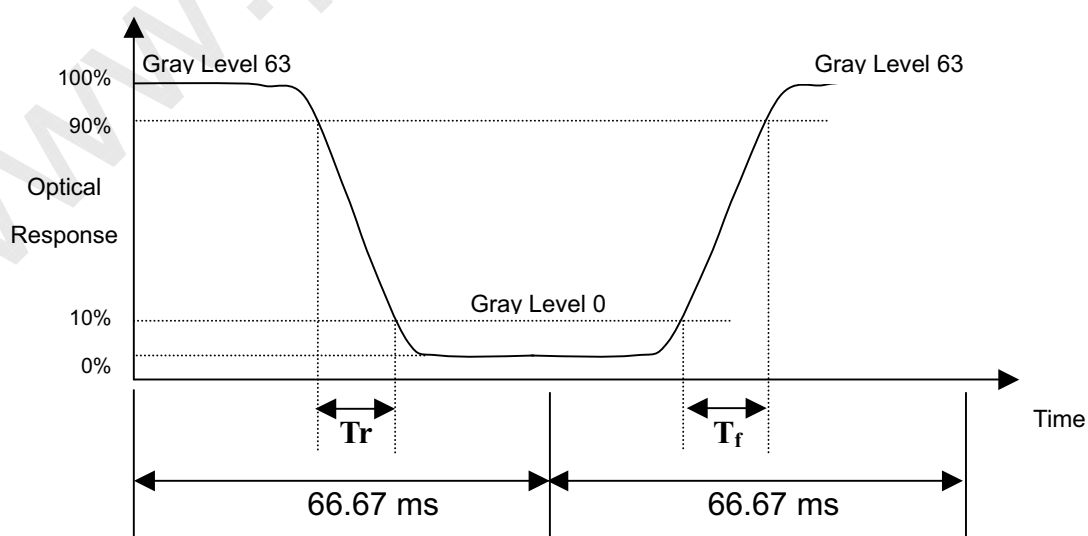
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

$$\text{CR} = \text{CR} (1)$$

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R , T_F):





Note (4) Definition of Average Luminance of White (L_{AVE}):

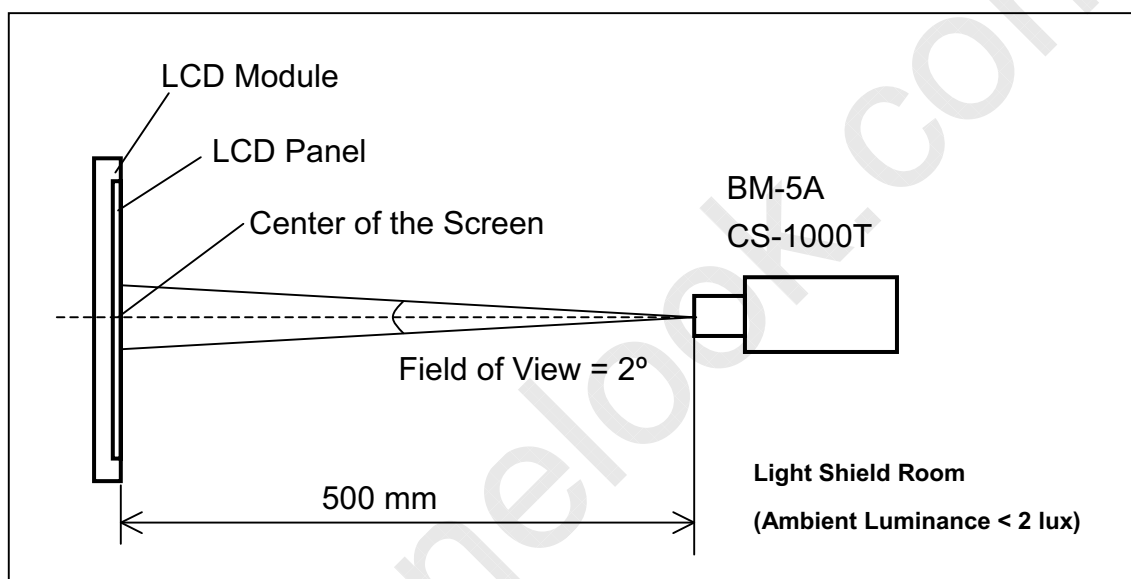
Measure the luminance of gray level 63 at 5 points

$$L_{AVE} = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (7).

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



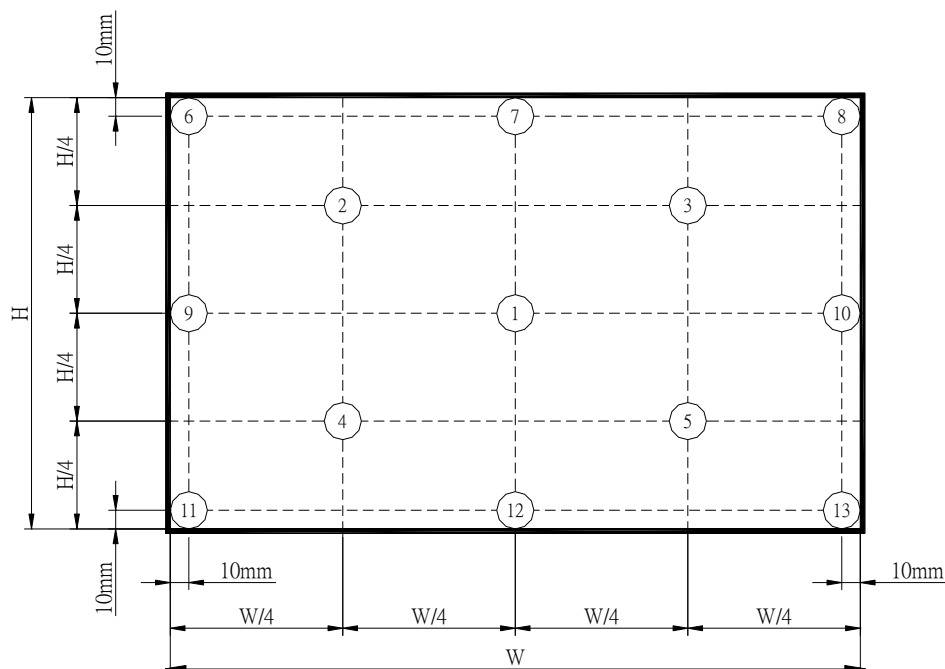


Note (6) Definition of White Variation ($\delta W_5, \delta W_{13}$):

Measure the luminance of gray level 63 at 5 points

$$\delta W_5 = \text{Minimum} [L(1), L(2), L(3), L(4), L(5)] / \text{Maximum} [L(1), L(2), L(3), L(4), L(5)]$$

$$\delta W_{13} = \text{Minimum} [L(1), L(2), \dots, L(12), L(13)] / \text{Maximum} [L(1), L(2), \dots, L(12), L(13)]$$



Note (7) Definition of color gamut (C.G%):

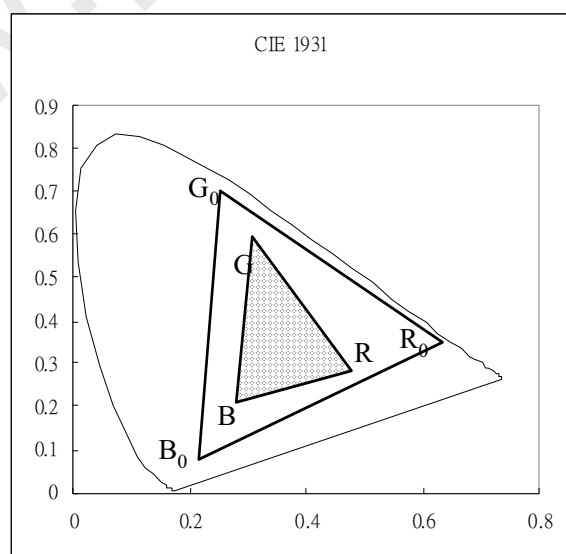
$$C.G\% = \Delta R G B / \Delta R_0 G_0 B_0 \cdot 100\%$$

R_0, G_0, B_0 : color coordinates of red, green, and blue defined by NTSC, respectively.

R, G, B : color coordinates of module on 63 gray levels of red, green, and blue, respectively.

$\Delta R_0 G_0 B_0$: area of triangle defined by R_0, G_0, B_0

$\Delta R G B$: area of triangle defined by R, G, B





8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

- (1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.
- (2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.
- (3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.
- (5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.
- (6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.
- (9) Do not disassemble the module.
- (10) Do not pull or fold the lamp wire.
- (11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

- (1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.
- (3) It may reduce the display quality if the ambient temperature is lower than 10 deg C. For example, the response time will become slowly, and the starting voltage of lamp will be higher than the room temperature.

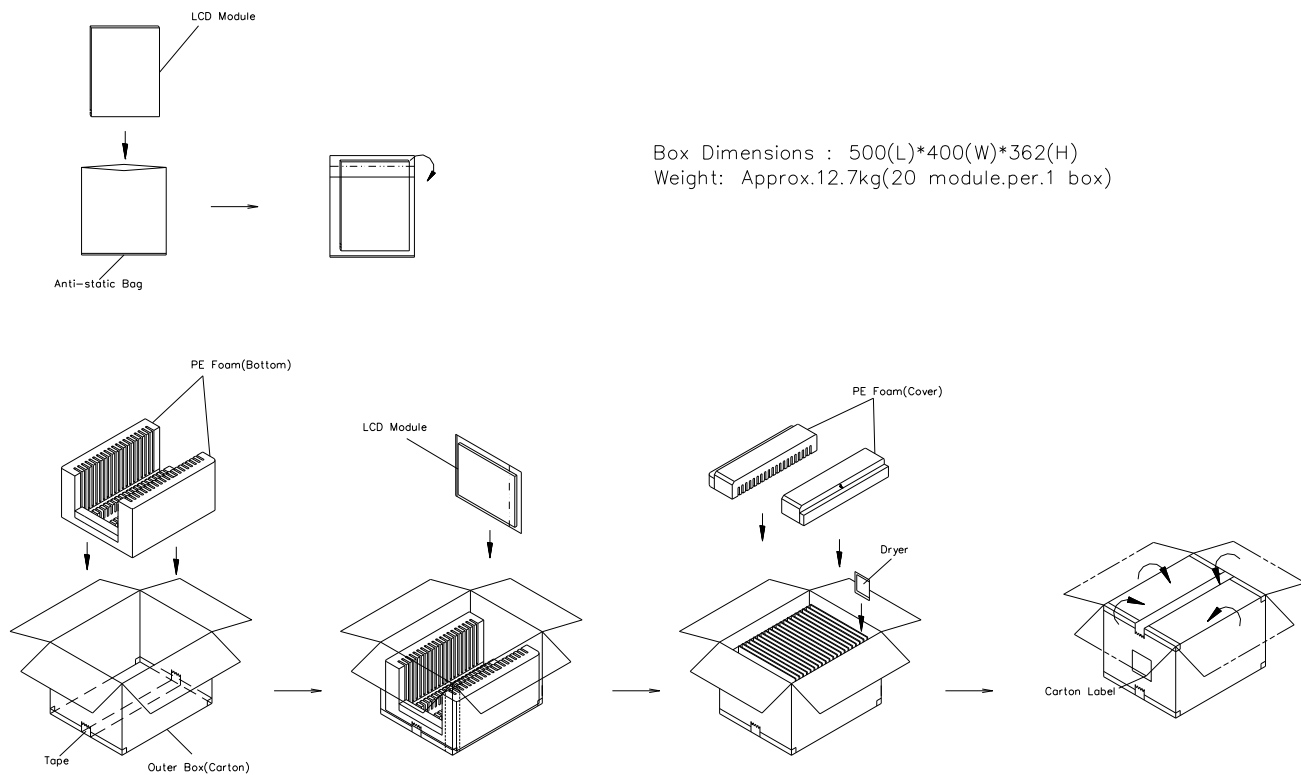
8.3 OPERATION PRECAUTIONS

- (1) Do not pull the I/F connector in or out while the module is operating.
- (2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.
- (3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.



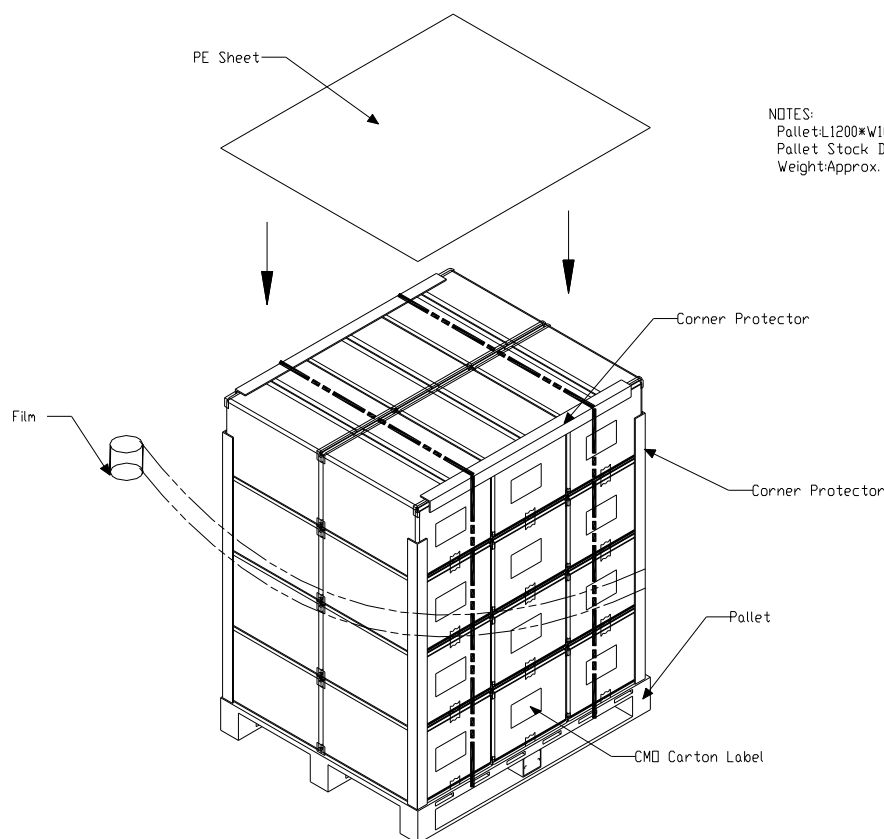
9.PACKING

9.1 CARTON





9.2 PALLET





10. DEFINITION OF LABELS

10.1 CMO MODULE LABEL

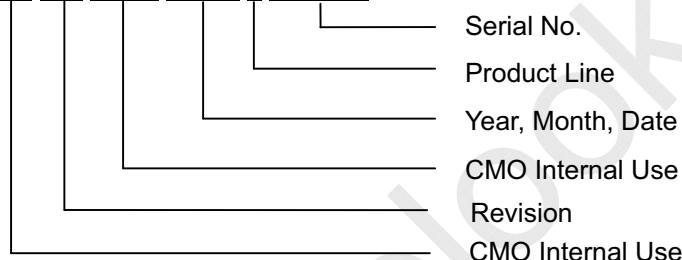
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: N150X3 - L0A

(b) Revision: Rev. XX, for example: C1, C2 ...etc.

(c) Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2001~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I, O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

For Lenovo's barcode content

11S PPPPPP Z1Z HHH SSSSSS YMM

(a) 11S: Fixed characters.

(b) PPPPPP (P/N): Customer part number 13N7068, fixed characters

(c) Z1Z: Fixed characters.

(d) HHH (Header Code): ABX


(e) SSSSSS: Series number.

(f) YMM: Y: The last character of year.

MM: Month



10.2 CARTON LABEL



CHI MEI OPTOELECTRONICS

PO.NO. _____

Part ID. P/N: 13N7068

Model Name N150X3-L0A

Carton ID. 26C43 25 4CN2142 Quantities _____

05/34 Year/Week Made in Taiwan

